In The Claims

1. (Amended) An intercom system for transferring audio information and data information among a plurality of users, the intercom system comprising:

a common, time-division-multiplexed parallel bus, wherein bandwidth on the bus is shared between digital audio data and inter-processor control messages;

a plurality of circuit modules connected to the bus, each one of the circuit modules being connected to at least one peripheral station for control message and audio data interface between the peripheral stations and the bus;

each circuit module having a control data communication circuit having a receiver and a transmitter, the transmitter having assigned transmit time slots for transferring inter-processor control messages onto the bus, the transmitter being configured for transmitting, in successive time slots, data identifying a unique address, each receiver being configured for distinguishing the address data received on the bus during a designated receive time slot for automatically determining which of the circuit modules is a source of a control message datum, such that no central processor controls data communications among the circuit modules.

2. (Amended) An intercom system for transferring audio information and data information among a plurality of users, the intercom system comprising:

a common, time-division-multiplexed parallel bus, wherein bandwidth on the bus is shared between digital audio data and inter-processor control messages;

a plurality of matrix cards connected to the bus, each matrix card having at least one intercom station connected to it for audio and control data interface between the stations and the bus;

each matrix card having a control data communication circuit having a receiver and a transmitter, the transmitter having assigned transmit time slots for transferring data onto the bus, the transmitter being configured for transmitting; in successive time slots, data identifying a unique address, each receiver being configured for distinguishing the address data received on the bus during a designated receive time slot for automatically determining which matrix cards are connected to the bus, such that no central processor controls data communications among the matrix cards.